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PTO/SB/05 (4/98)
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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 C.F.R. § 1.53(b))

Attorney Docket No.	22-0127
First Inventor or Application Identifier	Esmaell Yousefi
Title	See 1 in Addendum
Express Mail Label No.	EK432677139US

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

ADDRESS TO: Assistant Commissioner for Patents
Box Patent Application
Washington, DC 20231

1. [X] * Fee Transmittal Form *(e.g., PTO/SB/17)*
(Submit an original and a duplicate for fee processing)

2. [X] Specification [Total Pages 31]
(preferred arrangement set forth below)
- Descriptive title of the Invention
- Cross References to Related Applications
- Statement Regarding Fed sponsored R & D
- Reference to Microfiche Appendix
- Background of the Invention
- Brief Summary of the Invention
- Brief Description of the Drawings *(if filed)*
- Detailed Description
- Claim(s)
- Abstract of the Disclosure

3. [X] Drawing(s) *(35 U.S.C. 113)* [Total Sheets 4]

4. Oath or Declaration [Total Pages]
   a. [ ] Newly executed (original or copy)
   b. [ ] Copy from a prior application (37 C.F.R. § 1.63(d)) *(for continuation/divisional with Box 16 completed)*
      i. [ ] DELETION OF INVENTOR(S) Signed statement attached deleting inventor(s) named in the prior application, see 37 C.F.R. §§ 1.63(d)(2) and 1.33(b).

** NOTE FOR ITEMS 1 & 13 IN ORDER TO BE ENTITLED TO PAY SMALL ENTITY FEES, A SMALL ENTITY STATEMENT IS REQUIRED (37 C.F.R. § 1.27), EXCEPT IF ONE FILED IN A PRIOR APPLICATION IS RELIED UPON (37 C.F.R. § 1.28).*

5. [ ] Microfiche Computer Program *(Appendix)*

6. Nucleotide and/or Amino Acid Sequence Submission *(if applicable, all necessary)*
   a. [ ] Computer Readable Copy
   b. [ ] Paper Copy (identical to computer copy)
   c. [ ] Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

7. [ ] Assignment Papers (cover sheet & document(s))
8. [X] 37 C.F.R.§3.73(b) Statement *(when there is an assignee)* [X] Power of Attorney
9. [ ] English Translation Document *(if applicable)*
10. [ ] Information Disclosure Statement (IDS)/PTO-1449 [ ] Copies of IDS Citations
11. [ ] Preliminary Amendment
12. [X] Return Receipt Postcard (MPEP 503) *(Should be specifically itemized)*
13. [ ] * Small Entity Statement(s) *(PTO/SB/09-12)* [ ] Statement filed in prior application Status still proper and desired
14. [ ] Certified Copy of Priority Document(s) *(if foreign priority is claimed)*
15. [X] Other: Copy of Unsigned Declaration

16. **If a CONTINUING APPLICATION,** *check appropriate box, and supply the requisite information below and in a preliminary amendment:*
[ ] Continuation [ ] Divisional [ ] Continuation-in-part (CIP) of prior application No: _____/_____
Prior application information: *Examiner* _____ *Group / Art Unit:* _____
For CONTINUATION or DIVISIONAL APPS only: The entire disclosure of the prior application, from which an oath or declaration is supplied under Box 4b, is considered a part of the disclosure of the accompanying continuation or divisional application and is hereby incorporated by reference. The incorporation can only be relied upon when a portion has been inadvertently omitted from the submitted application parts.

17. CORRESPONDENCE ADDRESS

[ ] *Customer Number or Bar Code Label* *(Insert Customer No. or Attach bar code label here)* or [X] *Correspondence address below*

Name	Michael S. Yatsko				
	TRW Inc.				
Address	Law Dept.				
	One Space Park, Bldg. E2/6051				
City	Redondo Beach	State	CA	Zip Code	90245
Country	U.S.A.	Telephone	310-812-4910	Fax	310-812-2687

Name (Print/Type)	Michael Yatsko	Registration No. (Attorney/Agent)	28,135
Signature	Michael S Yatsko	Date	6/21/00

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Attachment to PTO/SB/05 (4/98) Utility Patent Application Transmittal

1. GATED POWER FOR A SATELLITE HOPPED DONWLINK WITH MULTIPLE PAYLOADS PER FRAME

Express Mail Mailing Label No. EK432677139US

Date of Deposit 6/21/00

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TRW Docket No. 22-0127

TITLE OF THE INVENTION

Gated Power for a Satellite Hopped Downlink with Multiple Payloads Per Frame

CROSS-REFERENCE TO RELATED APPLICATIONS

This application is related to TRW Docket No. 22-0006, titled "Gated Power Time Division Downlink for a Processing Satellite", filed March 16, 1999 as Serial No. 09/270,361.

BACKGROUND OF THE INVENTION

The present invention relates to satellite communications systems. In particular, the present invention relates to downlink beam power gating techniques particularly adapted to beam hopped multiple payload frame structures.

Satellites have long been used to provide communications capabilities on a global scale. Since

the inception of the modern communications satellite, however, one factor has remained constant: the limited availability of power on board the satellite. The limited availability of power persists today even in the face of tremendous advances in satellite technology.

Major drains on satellite power include the communications reception equipment used to receive the uplink and the transmission equipment used to generate the downlink. The transmission equipment in particular often requires 50% or more of the total power generated by a satellite. Furthermore, downlink power amplifiers are far from 100% efficient and therefore waste power whenever they are active.

Any undue drain on satellite power is undesirable. Thus, for instance, limitations on satellite power may prevent a satellite from encoding and decoding heavier and more error protective coding techniques. As another example, limited satellite power may reduce the number and type of observational or sensing functions which a satellite may perform.

In addition, as satellite technology has progressed, it has become more common for satellites to process their uplinks. In other words, the satellite may decode, process, route, queue, and otherwise manipulate data before recoding and packaging the data into downlink frames. Thus, the utilization of the downlink depends on the amount of data ready and waiting to be transmitted. Transmitting partially empty frames can be a waste of power, and can have detrimental impacts on the satellite performance through unnecessary servicing of queues, for example.

A need has long existed in the industry for a gated power time division downlink that addresses the problems noted above and others previously experienced.

BRIEF SUMMARY OF THE INVENTION

A preferred embodiment of the present invention provides a method for power gating a downlink beam

frame signal. The method includes the steps of transmitting, to form a single multiple payload frame, at least a first header signal, a first payload signal, a second header signal, and a second payload signal. When power gating is active, the method removes power from at least one of the first header signal and first payload signal in combination, and the second header signal and second payload signal in combination. The method for power gating may be extended to an N header N payload frame.

As an example, the method may also hop the downlink beam frame signal between at least two terrestrial cells. Then, power gating may be activated based in part on the terrestrial cell to which the downlink beam frame signal is currently hopped. In certain embodiments, the decision to power gate may be also based on a statistical multiplexing estimate of downlink frame utilization. As one example, when the downlink is expected to be 90% fully utilized, then power gating may occur for up to 10% of all frames. Power gating may also be performed in

order to maintain at least one data queue approximately at preselected occupancy level on average, or when too few cells are available to fill a frame or payload.

Another preferred embodiment of the present invention provides a power gating module for a downlink beam frame signal. The power gating module includes a power amplifier for amplifying, for transmission, frame signals that include at least a first header signal, a first payload signal, a second header signal, and a second payload signal. The power gating module further includes a power gating circuit coupled to the power amplifier. The power gating circuit includes a power gate input and is responsive to a power gating signal to remove power from at least one of the first header signal and first payload signal in combination, and the second header signal and second payload signal in combination before amplification by the power amplifier.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 illustrates a block diagram of a power gating module.

Figure 2 shows a detailed block diagram of a power gating module.

Figure 3 shows a modulator implementation that supports power gating.

Figure 4 shows a multiple payload frame signal with exemplary power gating control signals.

Figure 5 illustrates operational steps that occur before and after power gating a beam hopping multiple payload frame signal.

DETAILED DESCRIPTION OF THE INVENTION

Turning now to Figure 1, that figure shows a block diagram of a power gating module 100 that also functions, in general, to generate downlink frame

waveforms. The power gating module 100 includes a controller 102 and a waveform processing chain that operates on data provided by the data source 104 (which may be a data memory divided organized by data queues, for example). In particular, the waveform processing chain includes a waveform generator 106, a power amplifier 108, and a switch 110. The waveform processing chain further includes a first feed path 112 and a second feed path 114.

The first feed path 112 and the second feed path 114 may, for example, connect to individual antenna feed horns to direct spot beam coverage to distinct terrestrial cells. The feed paths 112-114 may also be characterized by a polarization effect on the waveform that propagates along the feed paths 112-114, including clockwise or counter-clockwise polarization.

The waveform generator 106 accepts baseband data from the data source 104 and creates a waveform to be transmitted (after amplification by the power amplifier 108). The switch 110 selects the particular

feed path 112-114 along which the waveform propagates (and thus, in certain embodiments, the polarization and/or hop location associated with the waveform).

The controller 102 exercises beam hopping and power gating control over the waveform to be transmitted. Thus, the controller 102 may output a power gating signal that is active when selected downlink frame signals are to be power gated. More particularly, as explained below, the controller 102 may power gate one or more header signals, payload signals, and flush signals based in part on the current hop location for a downlink beam and other criteria.

With regard to Figure 2, a more specific implementation of a power gating module 200 is shown. The power gating module 200 includes a data scheduler 202, a data router 204, and a waveform processing chain including a QPSK modulator 206, an upconverter 208, and a traveling wave tube amplifier (TWTA) 210. The switch 110 is illustrated in Figure 2 as a ferrite

switch 110 that directs the waveform to be transmitted through either the first feed path 112 or the second feed path 114.

Figure 2 also shows a control output 216 (that may used to carry, as examples, a power gating signal and a beam hopping selection signal), two frequency selection inputs 218 and 220 for the modulator 206 and the upconverter 208, a feed path selection input 222, and an intermediate waveform output 224 from the modulator. Preferably, additional ferrite switches 212 and 214 in the feed paths 112, 114 provide additional signal isolation (e.g., approximately 20db between input and output when the ferrite switch is off). In other words, the additional ferrite switches 212, 214 operate in response to the control output 216 to pass or block a waveform to be transmitted through the feed paths 112, 114. In other words, when the waveform to be transmitted is destined for the feed 112, then the ferrite switch 214 is coupled through the load 228 to ground. Similarly, when the waveform to be

transmitted is destined for the feed 114, then the ferrite switch 212 is coupled through the load 226 to ground.

During operation, the power gating module 200 accepts baseband data from the router 204 (e.g., an ATM cell router), and creates a waveform to be transmitted using the waveform processing chain. The waveform processing starts by directly converting baseband I and Q data to an intermediate frequency of, for example, 750 MHz. The waveform processing then selects one of F1 (e.g., 3.175 MHz) and F2 (e.g., 3.425) and one of F3 (e.g., 16 GHz) and F4 (e.g., 17.4 GHz) to produce a waveform to be transmitted with a final center frequency at one of 18.425 GHz, 18.675 GHz, 19.825 GHz, and 20.075 GHz. The scheduler 202 monitors the propagation of data through the waveform processing chain and determines when certain frame signals should be power gated. To that end, the scheduler 202 provides a power gating signal on the

control output 216 that is active when power gating is to occur.

The TWTA 210 amplifies the waveform to be transmitted, while the switch 110 determines along which feed path 112-114 (or additional feed paths) the amplified waveform will propagate. For this reason, the switch 110 includes the feed path selection input 222 responsive to information on the control output 216. Because the feed paths 112-114 are generally (though not necessarily) associated with feed horns that produce spot beams in geographically distinct terrestrial cells, the feed path selection input acts to determine the hop location of downlink frames. Thus downlink manifests itself as a beam spot that, typically, provides bandwidth for multiple terrestrial cells by hopping between them. The hop locations below are designated Even or Odd, but are not restricted to even or odd frames. Instead Even and Odd generally designate mutually exclusive time periods.

Turning next to Figure 3, that figure shows an implementation of the modulator 206 that supports power gating. Inphase data is supplied to the Inphase gate 302 while Quadrature data is supplied to the Quadrature gate 304. As illustrated, the Inphase and Quadrature gates 302, 304 are D flip flops with reset inputs. The Inphase and Quadrature gates 302, 304 feed a digital modulator core 306 that produces a modulated waveform on a modulator output 308. A local oscillator (LO) signal (preferably 750 MHz) provides an intermediate frequency carrier signal. The amplifier 310 boosts the modulated waveform, after which it is filtered by the bandpass filter 312. The bandpass filter 312 preferably has a passband centered at 750 MHz, for example, from 625 to 875 MHz.

A data clock 314 that preferably runs at 196.7 MHz drives the Inphase and Quadrature gates 304, 304. Note that a power gate input 316 connects to the Inphase and Quadrature gates 302, 304, as well as to the gating control input 318 of the digital modulator

core 306. When an active power gating signal is present on the power gate input 316, the Inphase and Quadrature gates 302, 304 have their outputs held in a known state (e.g., both 0). Furthermore, the digital modulator core 306 outputs a signal with frequency content outside of the passband of the bandpass filter 312.

For example, the digital modulator core 306 may output a DC signal in response to the active power gating signal. As a result, the bandpass filter eliminates the DC signal. A power gated signal results.

Returning to Figure 2, the upconverter 208 (e.g., a 20 GHz mixer) ordinarily outputs a fully upconverted signal for amplification and transmission. However, the absence of energy in the power gated signal causes the upconverter to produce substantially no signal at its output during power gating. As a result, the TWTA 210 does not expend amplification energy, and substantially no downlink energy is present in the

downlink beam while the power gating signal is active. In other words, the DC power consumption of the TWTA 210 is reduced by substantially eliminating radiated power.

Turning next to Figure 4, that figure presents a timing diagram 400 that illustrates a multiple payload frame signal 402 and power gating signals 404, 406, 408, 410, 412, 414, 416 (assumed active when high). As an example, the frame signal 402 may include a 368 symbol first header signal 418, a 7552 symbol first payload signal 420, a first 16 symbol flush signal 422, a 96 symbol second header signal 424, a 7552 symbol second payload signal 426, and a second 16 symbol flush signal 428. In general, however, the frame signal 402 may include N headers and N payloads independently subject to power gating.

The power gating signal 404 never goes active during the frame signal 402. Thus, none of the frame signals 418-428 are power gated. As a result, both first and second header signals 418, 424 and both

first and second payload signals 420, 426 are delivered to the ground. In contrast note that the power gating signal 416 is active across the entire frame signal 402. Thus, substantially no energy is provided in the downlink beam over the time during which the frame signal 402 would be transmitted.

On the other hand, the power gating signal 406 goes active during the second payload signal 426 and the second flush signal 428. Thus, the frame signal 402 continues to bear important overhead information in the first and second header signals 418, 424. The overhead information may include, for example, synchronization bits, beam hopping location identifiers, frame coding identifiers, frame counts, and the like.

The overhead information may further include power gating bit patterns that indicate to a ground receiver which frame signals are power gated. As an example, the first header signal 418 or second header signal 424 may include a frame type field that carries

repetitions of the bit pattern 10100101 to indicate power gating of the first payload signal 420 or second payload signal 426, or repetitions of the bit pattern 11110000 to indicate power gating of the entire frame signal 402. In particular, bit patterns may be assigned to identify any combination of header, payload, and flush signal power gating. Note also that a ground receiver may deactivate its own receivers in response to the bit patterns to save power during power gated sections of the frame signal.

Still with reference to Figure 4, the power gating signal 410 results in power gating of the first and second payload and flush signals 420, 422, 426, 428. Similarly, the power gating signal 412 results in power gating of the first payload signal 420 and the first flush signal 422.

Because the multiple payload frame signal 402 includes multiple headers, each preferably bearing synchronization information, additional power gating options are available. Thus, for example, the power

gating signal 408 power gates the second header signal 424, second payload signal 426, and the second flush symbols 428. Synchronization is nevertheless provided by the first header signal 418. Similarly, the power gating signal 414 power gates all the frame signals except for the first header signal 418.

The scheduler 202 may include logic to assert the power gating signal under many scenarios. For example, when the satellite moves into eclipse and less power is available, the scheduler 202 may power gate every other complete frame, every other payload, or any combination of frame signals to achieve a desired power reduction. As another example, the scheduler 202 may activate the power gating signal in response to a statistical multiplexing estimate of downlink beam utilization. As an example, if the downlink beam is estimated to be 90% utilized during a certain time period, then the scheduler 202 may power gate up to 10% of the frames or payloads. Such

estimates may be uplinked to the satellite or generated onboard.

As another example, the scheduler 202 may determine when to activate power gating based on the current terrestrial cell hop location of the downlink beam. Thus, scheduler 202 may power gate the second payload signal 426 if the bandwidth requirements of the current terrestrial cell are met by the first payload signal 420 alone. As yet another example, the scheduler 202 may power gate based on data queues present in the router 204. For example, a data queue from which ATM data cells are extracted to fill the second payload signal 426 may consistently have too few cells to completely fill the second payload signal 426. In response, the scheduler 202 may power gate the second payload signal 426 periodically in order to maintain the data queue approximately at preselected occupancy level, on average. In addition, an entire frame may be power gated when too few cells exist to fill one or more payloads in the frame.

Alternatively, only a selected one of the payloads may be power gated in such a case in order to maintain a selected minimum throughput.

Turning next to Figure 5, that figure shows a flow diagram 500 of the operational steps that occur before and after power gating. The operational steps include hopping 502 a downlink beam between at least two terrestrial cells. At step 504, queue statistics and traffic statistics are monitored and statistical multiplexing estimates of downlink utilization are obtained. At step 506, power gating is activated based on, as examples, beam hop locations, power saving goals, queue statistics and traffic statistics, and the like.

Continuing at step 508, one or more header signals, payload signals, and flush signals may be power gated. Thus, at step 510, a frame signal is transmitted in which at least one header signal, payload signal, or flush signal may have substantially no energy in the downlink beam.

Thus, the present invention provides selective power gating of frame signals in a beam hopped multiple payload downlink frame. The power gating may be responsive to many diverse criteria including power saving goals, queue statistics and traffic statistics, statistical multiplexing estimates, and terrestrial beam hop location. More efficient use of the downlink, satellite power, and satellite processing resources result.

While the invention has been described with reference to a preferred embodiment, those skilled in the art will understand that various changes may be made and equivalents may be substituted without departing from the scope of the invention. In addition, many modifications may be made to adapt a particular step, structure, or material to the teachings of the invention without departing from its scope. Therefore, it is intended that the invention not be limited to the particular embodiment disclosed,

but that the invention will include all embodiments falling within the scope of the appended claims.

What is claimed is:

1. A method for power gating a downlink beam frame signal, the method comprising:

transmitting, to form a single frame, at least a first header signal, a first payload signal, a second header signal, and a second payload signal;

when a power gating signal is active, removing RF power from at least one of the first header signal and first payload signal in combination, and the second header signal and second payload signal in combination, thereby reducing DC power consumption.

2. The method of claim 1, further comprising hopping the downlink beam frame signal between at least two terrestrial cells.

3. The method of claim 2, further comprising the step of activating the power gating signal based on the terrestrial cell to which the downlink beam frame signal is currently hopped.

4. The method of claim 1, further comprising the step of activating the power gating signal based on a statistical multiplexing estimate of downlink frame utilization.

5. The method of claim 1, further comprising the step of activating the power gating signal in order to maintain at least one data queue on average approximately at preselected occupancy level.

6. The method of claim 1, further comprising the step of transmitting a first flush signal and a second flush signal, and wherein removing power comprises removing power from at least one of the first header signal, first payload signal, and first flush signal in combination, and the second header signal, second payload signal, and second flush signal in combination.

7. The method of claim 1, wherein removing power for the first header signal, the first payload signal, the second header signal, and the second payload signal.

8. The method of claim 1, wherein removing power comprises removing power from the first payload signal, the second header signal, and the second payload signal.

9. The method of claim 1, wherein removing power comprises removing power from the first header signal, the first payload signal, and the second payload signal.

10. The method of claim 1, wherein transmitting comprises transmitting to form a single frame a first header signal, a first payload signal, a second header signal, a second payload signal, at least one additional header signal, and at least one additional payload signal;

when the power gating signal is active, removing power from at least one of the first header signal and first payload signal in combination, the second header signal and second payload signal in combination, and the additional header signal and the additional payload signal in combination.

11. A power gating module for power gating a downlink beam frame signal, the power gating module comprising:

a power amplifier for amplifying for transmission frame signals including at least a first header signal, a first payload signal, a second header signal, and a second payload signal;

a power gating circuit coupled to the power amplifier, the power gating circuit including a power gate input and responsive to a power gating signal to remove power from at least one of the first header signal and first payload signal in combination, and the second header signal and second payload signal in combination before amplification by the power amplifier.

12. The power gating module of claim 11, wherein the power gating circuit comprises a digital modulator with a gating control input connected to the power gate input and a bandpass filter with a predetermined passband coupled to a modulator output of the digital modulator.

13. The power gating module of claim 12, wherein the digital modulator outputs a modulated signal with frequency content outside the passband in response to the power gating signal.

14. The power gating module of claim 13, wherein the frequency content is substantially DC frequency content.

15. The power gating module of claim 12, wherein the digital modulator is a QPSK modulator and further comprising an Inphase gate and a Quadrature gate coupled to the digital modulator.

16. The power gating module of claim 15, wherein the Inphase gate and the Quadrature gate are held in a known output state in response to the power gating signal.

17. The power gating module of claim 11, wherein the power gating signal is active during the first header signal, the first payload signal, the second header signal, and the second payload signal.

18. The power gating module of claim 11, wherein the power gating signal is active during the first payload signal, the second header signal, and the second payload signal.

19. The power gating module of claim 11, wherein the power gating signal is active during the first header signal, the first payload signal, and the second payload signal.

20. The power gating module of claim 11, comprising:

a switch coupled to the power amplifier, the switch including a feed path selection input;

a first feed path coupled to the switch and characterized by a first hop location; and

a second feed path coupled to the switch and characterized by a second hop location.

21. The power gating module of claim 20, wherein the switch is a ferrite switch.

22. The power gating module of claim 20, wherein the power gating signal is active based in part on the feed path selection of the first hop location or the second hop location.

23. A power gated frame signal comprising:

a single frame comprising at least a first header signal, a first payload signal, a second header signal, and a second payload signal,

wherein at least one of the first header signal and first payload signal in combination, and the second header signal and second payload signal in combination is power gated.

24. The power gated frame signal of claim 23, wherein the single frame further comprises at least one additional header signal, and at least one additional payload signal, and

wherein at least one of the first header signal and first payload signal in combination, the second header signal and second payload signal in combination, and the additional header signal and the

additional payload signal in combination is power gated.

25. The power gating module of claim 23, wherein the first header signal, the first payload signal, the second header signal, and the second payload signal are power gated.

26. The power gating module of claim 23, wherein the first payload signal, the second header signal, and the second payload signal are power gated.

27. The power gating module of claim 23, wherein the first header signal, the first payload signal, and the second payload signal are power gated.

Gated Power for a Satellite Hopped Downlink with Multiple Payloads Per Frame

ABSTRACT OF THE DISCLOSURE

A power gating module (200) for a downlink beam frame signal (402) includes a power amplifier (210) for amplifying for transmission frame signals that include at least a first header signal (418), a first payload signal (420), a second header signal (424), and a second payload signal (426). The power gating module (200) further includes a power gating circuit (300) coupled to the power amplifier (210). The power gating circuit (300) includes a power gate input (318) and is responsive to a power gating signal to remove power from at least one of the first header signal (418) and first payload signal (420) in combination, and the second header signal (424) and second payload signal (426) in combination before amplification by the power amplifier (210).

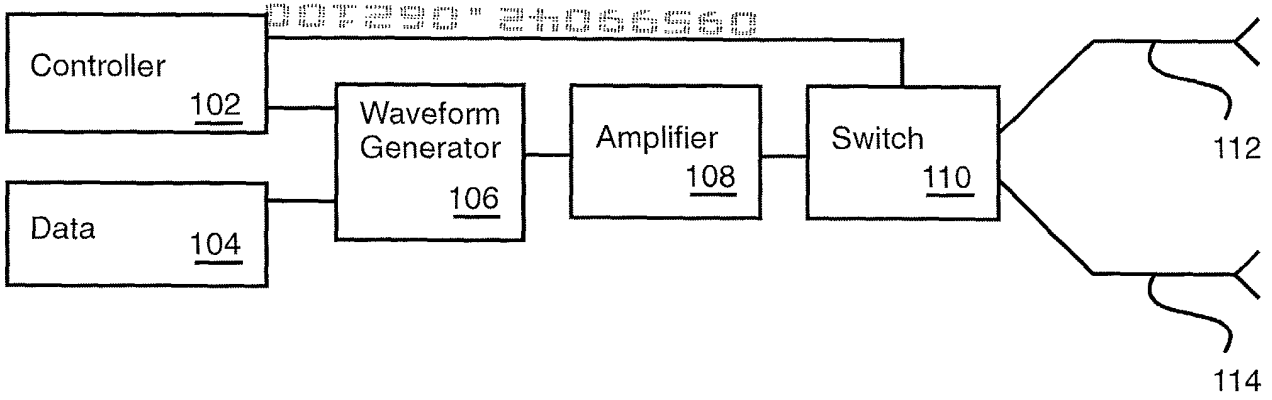
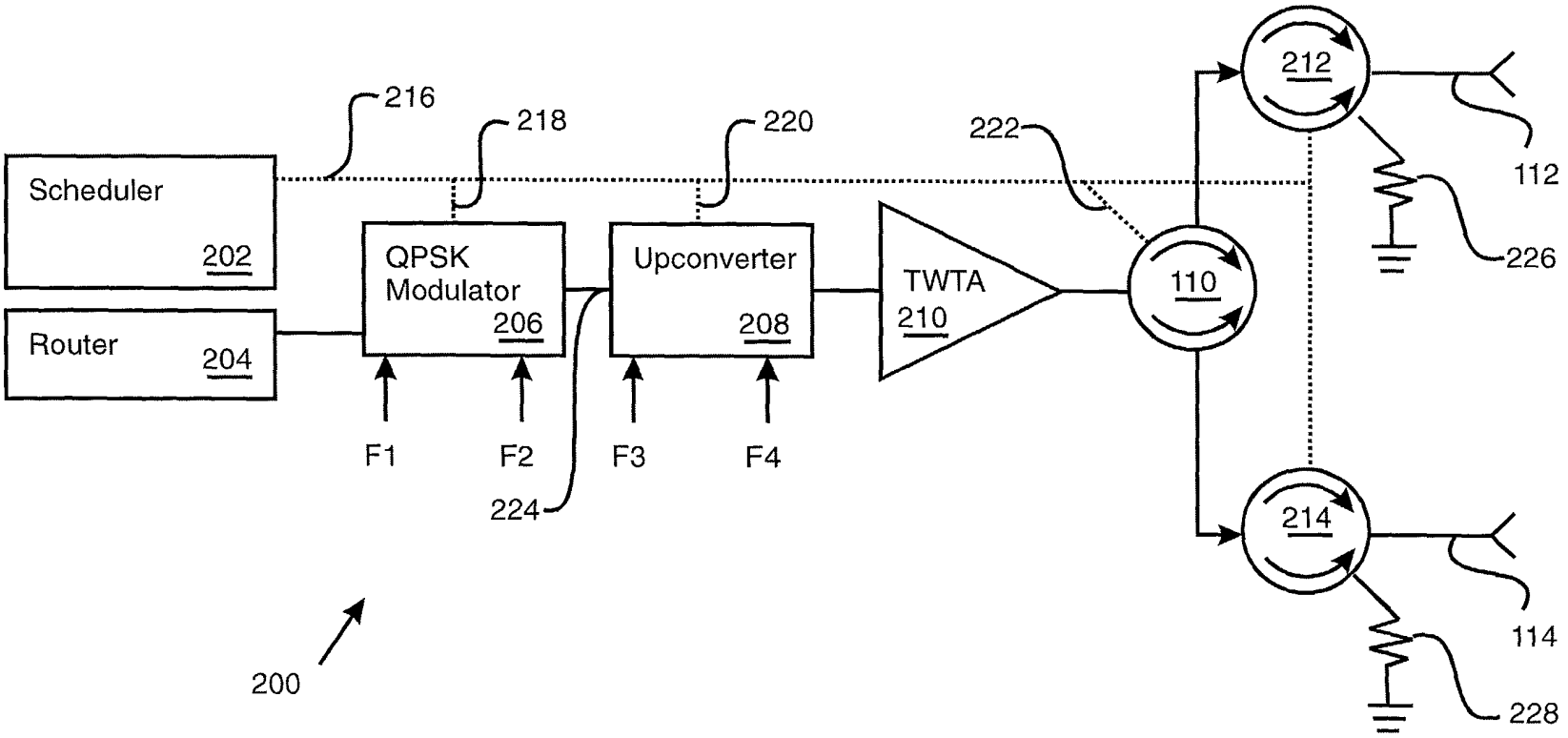


Figure 1

100



200

Figure 2

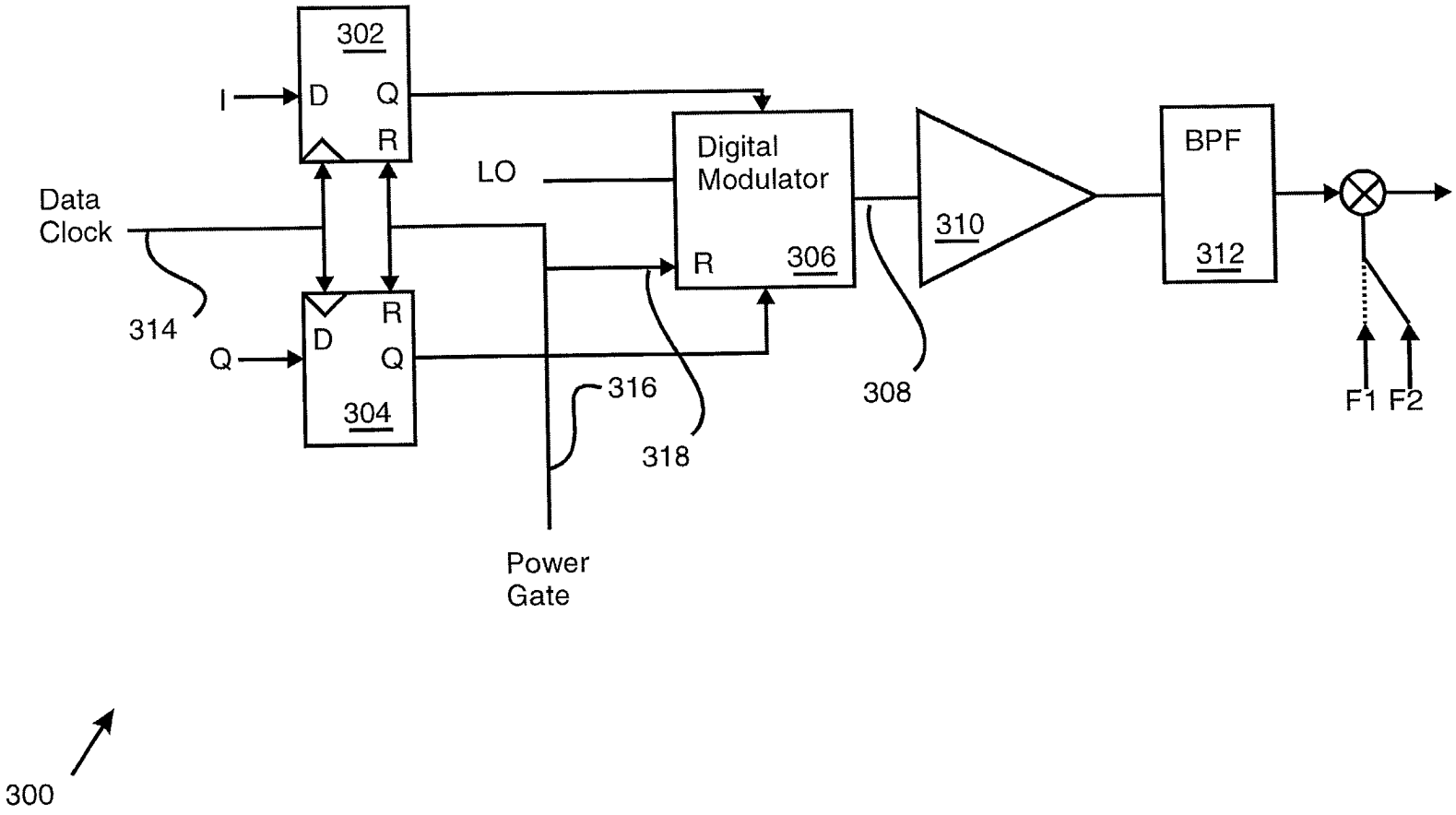


Figure 3

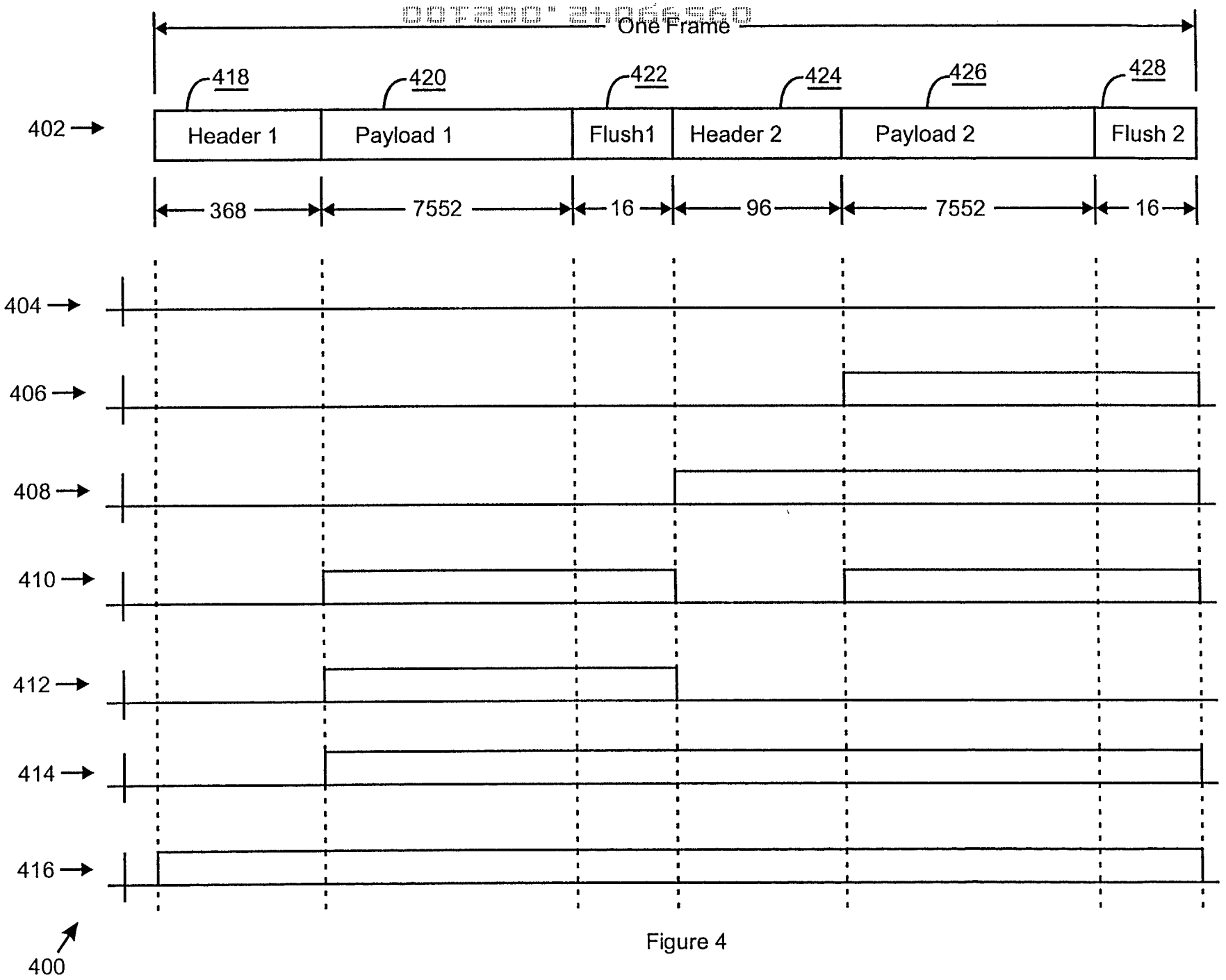

One Frame
418
420
422
424
426
428
402
Header 1
Payload 1
Flush1
Header 2
Payload 2
Flush 2
368
7552
16
96
7552
16
404
406
408
410
412
414
416
400

Figure 4

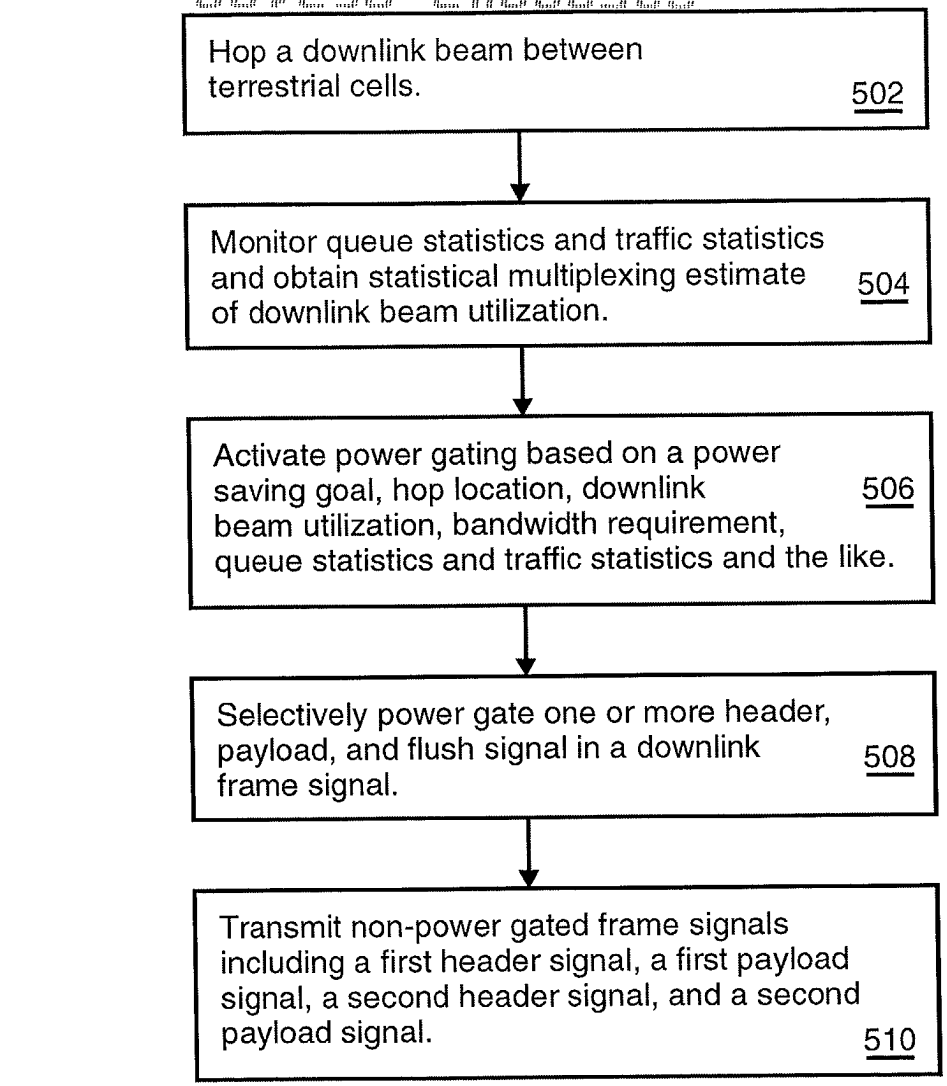

Hop a downlink beam between terrestrial cells. 502
Monitor queue statistics and traffic statistics and obtain statistical multiplexing estimate of downlink beam utilization. 504
Activate power gating based on a power saving goal, hop location, downlink beam utilization, bandwidth requirement, queue statistics and traffic statistics and the like. 506
Selectively power gate one or more header, payload, and flush signal in a downlink frame signal. 508
Transmit non-power gated frame signals including a first header signal, a first payload signal, a second header signal, and a second payload signal. 510
500

Figure 5

Docket No. 22-0127

DECLARATION FOR PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name,

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled **GATED POWER FOR A SATELLITE HOPPED DOWNLINK WITH ULTIPLE PAYLOADS PER FRAME** the specification of which

_____ is attached hereto

_____ was filed on _____ as Application Serial No. _____ and was amended on _____.
(if applicable)

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, §1.56(a).

I hereby claim foreign priority benefits under Title 35, United States Code, §119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)			Priority Claimed	
NONE				
(Number)	(Country)	(Day/Mo./Yr. Filed)	Yes	No

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I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, §1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

NONE			
(Number)	(Country)	(Day/Mo./Yr. Filed)	(Status)

I hereby appoint as principal attorneys:

Robert W. Keller, Reg. No. 25,347
Michael S. Yatsko, Reg. No. 28,135
Connie M. Thousand, Reg. No. 43,191
William M. Wesley, Reg. No. 26,521

each with full power to prosecute this application, to transact all business in the United States Patent and Trademark Office connected therewith, and to appoint and revoke associate and substitute associate attorneys.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Address all telephone calls to: (310) 812-4910

Address all correspondence to: PATENT COUNSEL
TRW Inc.
Space & Electronics Group
One Space Park, E2/6051
Redondo Beach, California 90278

Full name of first inventor Esmaell (NMI) Yousefi

Inventor's signature _____ Date: _____

Residence Manhattan Beach, California

Citizenship United States

Post Office Address 740 12th Street, #A, Manhattan Beach, California 90266

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Full name of second inventor Stuart T. Linsky
Inventor's signature _____ Date: _____
Residence San Pedro, California
Citizenship United States
Post Office Address 1070 Santa Cruz Street, San Pedro, California 90732

Full name of third inventor Mark E. Bever
Inventor's signature _____ Date: _____
Residence Redondo Beach, California
Citizenship United States
Post Office Address 208 Vista del Parque, Redondo Beach, California 90277

Full name of fourth inventor Fred C. Tramm
Inventor's signature _____ Date: _____
Residence Rancho Palos Verdes, California
Citizenship United States
Post Office Address 4927 Golden Arrow Drive, Rancho Palos Verdes, California 90275

Full name of fifth inventor Lisa A. Moy-Yee
Inventor's signature _____ Date: _____
Residence Torrance, California
Citizenship United States
Post Office Address 3861 Meadow Park Lane, Torrance, California 90505

Full name of sixth inventor Vincent (NMI) Nguyen
Inventor's signature _____ Date: _____
Residence Garden Grove, California
Citizenship United States
Post Office Address 11902 Sumo Circle, Garden Grove, California 92840

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Full name of seventh inventor Gefferie H. Yee-Madera

Inventor's signature _____ Date: _____

Residence San Gabriel, California

Citizenship United States

Post Office Address 1223 Euclid Avenue, San Gabriel, California 91776